Remarks/Arguments

In a Final Office Action dated December 12, 2006, claims 1-36 were rejected under § 103 over Considine in view of Pham. Applicants respectfully traverse the rejections and submit that the claims are allowable.

Section 103 Rejections

The Final Office Action admitted that Considine did not show an embedded processor or a frame classifier. For those elements reference was made to selected elements in Pham. The Final Office Action did state that Considine did show dedicated hardware assist circuitry. Applicants respectfully traverse the showing of dedicated hardware assist circuitry in Considine, the frame classifier in Pham and the proposed combination of Considine and Pham.

The Office Action indicated that the dedicated hardware assist circuitry was hardware of the port processors to perform selected port processing functions, referencing paragraphs 77 and 79 of Considine. Using claim 19 as exemplary, each port processor is to include dedicated hardware assist circuitry to perform first selected port processing functions. The Office Action directs attention to paragraphs 77 and 79 as the first selected port processing functions and cites unspecified hardware in the port processor, the port processors being defined as the IP processors 102 and SP processors 104. Applicants submit that this is an improper rejection. Paragraph 77 very broadly discusses functions performed by the IP or SP processors 102 or 104 as a whole. There is no indication whatsoever that any alleged, unspecified hardware in the IP or SP processors performs these functions. Indeed, Applicants submits that it cannot be shown as the IP and SP processors 102 and 104 are actually only logical items, not actual port processors as required by the claim. Fig. 2 is the hardware environment to develop the logical view of Fig. 1 and Considine does not provide any correspondence between the IP and SP processors and any elements shown in Fig. 2.

Applicants thus submit that the Office Action is improper by failing to provide specific citation to dedicated hardware assist circuitry.

Applicants also traverse the rejection based on Pham. The Office Action first errs in correspondence of the port processors, citing elements 40 and 50. Element 40 is the

switch fabric, not a port processor. Element 50 is the entire protocol processor itself including a switch fabric 56, ingress processors 52, egress processors 54, data processors 58 and control processors 60. Element 50 is not properly corresponded to a port processor of claim 19.

The Office Action next corresponds data processors 42 and 44 to be the required embedded processors. Applicants submit this correspondence is again improper. Port processors are required to have a node to receive and transmit network traffic. In Pham such nodes are connected to ingress or egress processors, not data processors. The data processors are separated from the ingress and egress processors by a switch fabric. The data processors 42, 44 are akin to the back end processors MIC 136, LIO 138 and SIO 140 in Considine, which correspondence has been admitted as being erroneous by the withdrawal of the prior rejection. Putting it another way, if the data processors 42 and 44 are the embedded processors in the port processor, then the entire device in Pham has been equated to be a single port processor, which is directly opposed to the teachings of Pham. Further, one skilled in the art would never combine Pham and Considine as would effectively be required by the Office Action. The actual designs of Considine and Pham are highly equivalent so that they are replacements at the higher level, not combinable where Pham would be treated as a port processor in Considine. Applicants submit that the correspondence of the data processors is erroneous and the entire combination of Pham and Considine as would be required would not be made by one skilled in the art.

The Office Action corresponds the frame classifier to be the ingress processors 30 and 34 of Pham. This correspondence highlights the error of the embedded processor correspondence of the data processors 42, 44. The claim language for the frame classifier is – "a frame classifier to determine if said network traffic should be provided to said embedded processor or directly to said switch." Referring to Pham, the only way to provide network traffic from the ingress processor to the data processor is through the switch fabric 40. Yet the claim language clearly indicates that providing the network traffic to the embedded processor or the switch are alternatives, not the same operation as would be required in Pham. Therefore the correspondence of the various elements of Pham to claim 19 is shown to be further in error.

In view of the numerous errors and improper items being corresponded, Applicants submit that the rejection is improper and must be withdrawn.

Claims 21-24 require second, and in some cases third, embedded processors included in each port processor. The Office Action reference to other data processors in Pham is improper for the same reasons as above and as exemplified by the requirement in the claims that the frame classifier determine if the network traffic should be provided to the second embedded, in addition to the first embedded processor or directly to the switch. As the additional data processors in Pham are also across the switch from the ingress processors, the error above is only exacerbated so that the improper nature of the rejection becomes apparent.

Equivalent arguments apply to the relevant claims in claims 1-18 and 28-36. As such, Applicants submit that the claims were, and are, allowable over Considine and Pham.

Conclusion:

Reconsideration of the pending claims in light of the above remarks is respectfully requested. Allowance of all of the claims is submitted as being proper.

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